REMARKS

In the Office Action, the Examiner objected to the specification because the abstract exceeded 150 words in length. The abstract has been amended. Applicants respectfully request that the Examiner's objection to the specification be withdrawn.

Claims 1-37 are pending in the present application. In the Office Action, claims 1-37 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-37 of U.S. Patent No. 6,823,433. In the interest of expediency, Applicant has included herein a terminal disclaimer and respectfully requests that the Examiner's rejection of claims 1-37 be withdrawn. However, it will be appreciated that the filing of the terminal disclaimer to obviate the Examiner's rejection is not an admission of the propriety of the rejection. *Quad Environmental Technologies Corp. vs. Union Sanitary District*, 946 F.2d 870, 20 USPQ2d 1392 (Fed Cir. 1991). See, *e.g.*, MPEP §804.03.

In the Office Action, claims 1-9, 11-13, 23, 32, and 36-37 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Maruyama, et al (U.S. Patent No. 6,052,763). Claims 10, 20, 22, 26, and 35 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Maruyama in view of admitted prior art. The Examiner's rejections are respectfully traversed.

Independent claims 1, 11-13, 23, and 32 set forth techniques for managing a memory for storing data arranged within a plurality of memory pages. Claims 1, 11-13, 23, and 32 set forth, among other things, receiving a linear address generated during execution of a current instruction and using the linear address to access at least one security attribute data structure located in the memory to obtain a security attribute of a selected memory page. Claims 1, 11-13, 23, and 32 also set forth comparing a numerical value conveyed by a security attribute of the current

instruction to a numerical value conveyed by the security attribute of the selected memory page and producing an output signal dependent upon a result of the comparison.

Maruyama describes a system bus interface unit 16 that receives memory access requests from a system bus 15 and sends access data to a dynamic random access memory (DRAM) 19. The access addresses are stored in a decoder 21 while a bus master identification is sent to, and stored in, a register 22. The decoder 21 uses a flag bit to identify whether an access address is for a conventional address space or an atomic address space. If the access address is for an atomic address space, the register 22, comparator 23, and bus master identification table 24 determine if the requesting bus master has privileges for performing an atomic transaction. In particular, the comparator 24 accesses addresses from the register 22 and the bus master identification table 24. The comparator 24 then compares the accessed addresses. See Maruyama, col. 5, line 19 – col. 6, line 41 and Figure 1.

However, Maruyama does not describe or suggest using a linear address to access at least one security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Maruyama and request that the Examiner's rejections of claims 1-9, 11-13, 23, 32, and 36-37 under 35 U.S.C. 102(b) be withdrawn.

Moreover, it is respectfully submitted that the pending claims are not obvious in view of Maruyama or the admitted prior art. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Maruyama fails to describe or suggest using a linear address to access at least one security attribute data structure

located in a memory to obtain a security attribute of a selected memory page in the memory, as set forth in independent claims 1, 11-13, 23, and 32. The Examiner relies upon the admitted prior art to describe the use of a user/supervisor bit and a read/write bit. However, the admitted prior art fails to remedy the aforementioned fundamental deficiencies of the primary reference.

The cited references also fail to provide any suggestion or motivation to modify the prior art to arrive at Applicants' claimed invention. To the contrary, Maruyama teaches away from the present invention. In particular, Maruyama teaches that unauthorized bus masters should not be permitted to access the dynamic random access memory 19 under certain circumstances. Accordingly, Maruyama teaches that the bus master identifier table 24 should be hosted in an EEPROM or battery backup RAM that is separate from the DRAM 19. See Maruyama, col. 5, ll. 34-35. Maruyama therefore teaches away from using a linear address to access at least one security attribute data structure located in a memory to obtain a security attribute of a selected memory page in the memory. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine*, 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

For at least the aforementioned reasons, Applicants respectfully submit that the Examiner has failed to make a *prima facie* case that the present invention is obvious over Maruyama and the admitted prior art, either alone or in combination. Applicants request that the Examiner's rejections of claims 10, 20, 22, 26, and 35 under 35 U.S.C. 103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the

undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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